

## 53.4: Novel Pulsed Drive Scheme for Improved Gray-Level Uniformity of Large-Area Cholesteric Displays

Duane Marhefka, Nithya Venkataraman, Asad Khan, Sankar Barua, Forrest Nicholson, Todd Ernst, and J. William Doane

Kent Displays, Inc., 343 Portage Blvd., Kent, Ohio 44240, USA

### Abstract

A new drive scheme is presented for producing uniform grays over large-area, low-resolution cholesteric liquid crystal displays. Gray-level sensitivity to display non-uniformities is minimized, which simplifies display manufacturing. While applicable to both rigid and flexible displays, the impact on flexible displays will be particularly important with roll to roll manufacturing capability coming online.

### 1. Introduction

Bistable cholesteric liquid crystal displays (ChLCDs) are reflective displays with a simple structure that require neither polarizers, compensation films, nor backlights.<sup>[1,2]</sup> Their zero-power image retention and sunlight readability have led to their integration into numerous signage and battery-powered applications. Most of these applications to date have employed rigid glass-based monochrome displays with binary (on/off) image content. However, both grayscale and stacked full color operation have been demonstrated.

Recent technology advances have permitted manufacture of flexible ChLCDs on plastic substrates by encapsulating the liquid crystal.<sup>[3,4,5]</sup> The new flexible displays based on the phase separation approach to encapsulation are manufactured with a simple lamination process and may be cut into interesting shapes after assembly. These displays have all the features of the standard cholesteric technology, such that full color may be achieved by stacking multiple layers each tuned to reflect a different wavelength. Highly flexible full color displays using ultra thin substrates and conducting polymer electrodes have already been demonstrated.<sup>[6]</sup> Compelling new applications are being developed in which these displays are addressed at very low resolution, perhaps even as a single pixel. These new applications demand the ability to produce uniform gray levels across the entire display area.

Producing uniform gray levels can prove difficult, as imperfections in the display that are typically hidden in binary (on/off) driving reveal themselves when driving to gray levels. Because very low resolution displays are considered, large areas are required to have a uniform appearance. There is no image content to assist in hiding the imperfections.

In this work, a new drive scheme is presented for cholesteric liquid crystal displays. The approach makes use of the cumulative effect of cholesteric displays, but in a manner different from the drive technique known as cumulative drive.<sup>[7]</sup> The scheme is applicable to displays built on both glass and flexible plastic substrates. The drive scheme minimizes the sensitivity of the gray levels to display imperfections and reduces the need for further improvements in display manufacturing processes. This enables new applications such as large area architectural tiles.

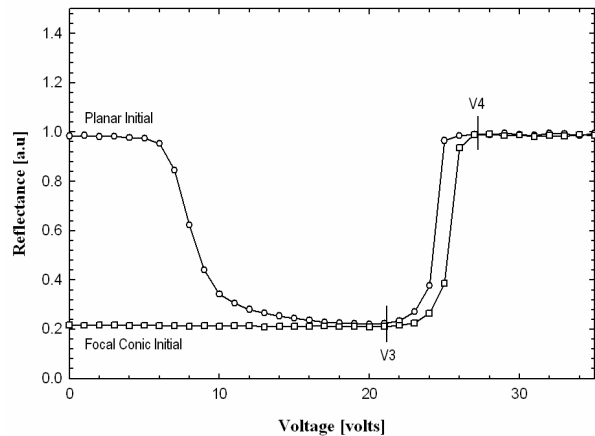


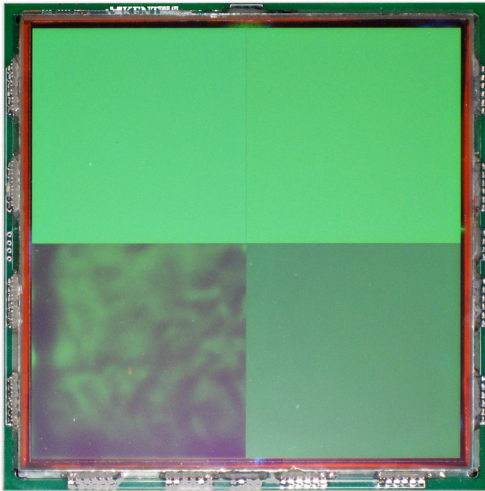
Figure 1: Voltage Response Curve for 100 ms Conventional Drive Pulses (5  $\mu\text{m}$  cell gap).

### 2. Typical Approaches to Grayscale

A typical drive scheme for cholesteric displays involves erasing the display to either a planar (bright) or focal conic (dark) texture and then driving the display to its desired brightness with a single drive pulse. Figure 1 illustrates the resultant reflectance of driving a typical cholesteric material with a 100 ms pulse (frequency = 250 Hz) from either the full planar or focal conic initial textures. The horizontal axis shows the root mean square (rms) voltage of the applied pulse, while the vertical axis shows the resultant reflectance normalized to a peak value of 1.

A drive pulse with rms voltage slightly less than or equal to  $V_3$  may be used to drive a pixel dark and with rms voltage  $\geq V_4$  may be used to drive a pixel bright. Gray levels are achieved by applying a drive pulse with an rms value between  $V_3$  and  $V_4$ . The rms values between  $V_3$  and  $V_4$  may be achieved directly using amplitude modulation (AM) of the applied pulse. However, it is often desirable to achieve the rms value by implementing a pulse-width modulation (PWM) approach that selects between two voltage levels near  $V_3$  and  $V_4$ . Such a PWM approach simplifies drive electronics by eliminating the need to drive to arbitrary voltage levels.

These typical AM and PWM approaches have proven unsatisfactory at producing uniform gray levels over large-area pixels. Figure 2 illustrates a 13 cm x 13 cm glass display (9  $\mu\text{m}$  cell gap) composed of 2 rows and 2 columns of directly driven pixels. The bottom left pixel of the display has been driven from the focal conic state with a 41.5V square wave drive pulse of 100 ms duration and frequency of 250 Hz. The uniformity problem is clearly exhibited in this pixel, while the top two pixels that have been driven fully planar exhibit no uniformity problems.



**Figure 2: Display Illustrating Planar (top), Typical Gray (bottom left), and New Gray (bottom right).**

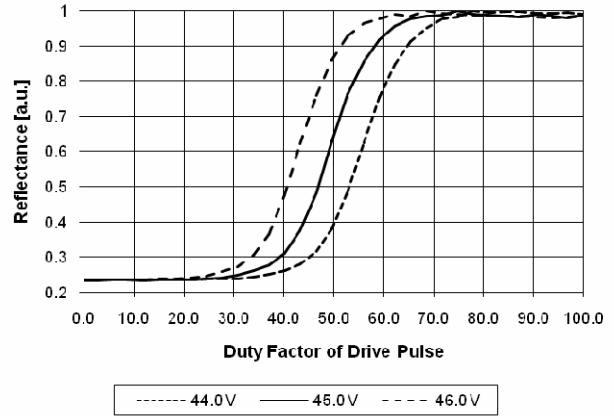
Analysis of the voltage response curve of Figure 1 provides some insight into the non-uniform results of the conventional approach. It must first be noted that the liquid crystal material responds to the electric field across it rather than to the voltage of the applied pulse. The electric field is related to the voltage of the applied pulse, but also depends on the cell gap as well as the dielectric constants of the liquid crystal and any polymer structures within the cell. Thus, gray level sensitivity to voltage is also an indication of sensitivity to imperfections in cell thickness or internal structure. Figure 1 illustrates a high sensitivity of reflectance to drive voltages between V3 and V4 for a 100 ms drive pulse. Thus, the display is very sensitive to imperfections when driven in such a manner.

Such sensitivity has also been demonstrated with the PWM drive scheme. Figure 3 illustrates results from a PWM drive scheme that used two voltages, designated V0 and V2. The duty factor gives the percentage of the drive pulse in which the V0 voltage is driven. Note that the V2 voltage is equal to 0.75 times V0. Considering the nominal case of V0 = 45.0V, a high duty factor results in a planar (bright) pixel and a low duty factor results in a focal conic (dark) pixel. It is clear from the figure that at high and low duty factors small changes of ±1V in V0 don't affect reflectance. However, at the 50% duty factor used to drive a midlevel gray the error is quite large.

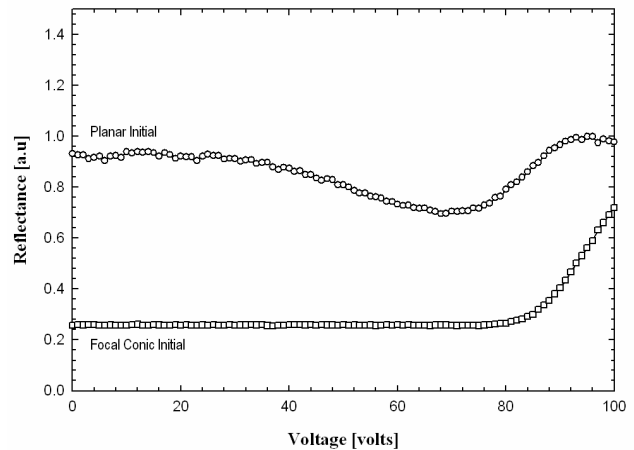
### 3. New Pulsed Approach to Grayscale

The new drive scheme differs from the conventional approach in that multiple drive pulses are used to achieve most gray levels and that driving makes use of the left side of the voltage response curve. Many characteristics of the display system are taken advantage of in the approach. These include the relative insensitivity of the display to voltage for short drive pulses, the cumulative effect of cholesteric displays, and the use of a direct drive architecture.

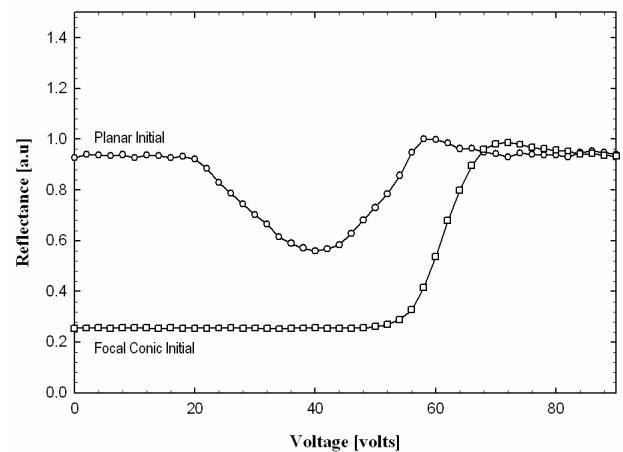
Figures 4 and 5 illustrate the resultant reflectance of driving a typical cholesteric material with 0.5 ms and 1.0 ms drive pulses, respectively, from both the full planar and focal conic initial textures. The slopes of the curves are much lower than for the 100 ms drive pulse in Figure 1. This indicates that the reflectance



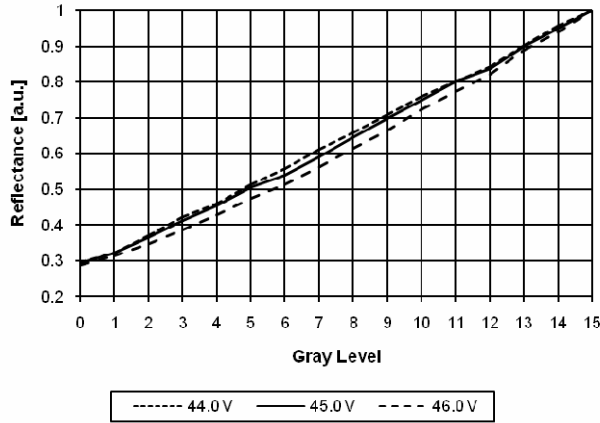
**Figure 3: Voltage Sensitivity for Conventional 1.95 ms PWM Drive Pulses (cell gap = 5.0 μm).**



**Figure 4: Voltage Response Curve for 0.5 ms Conventional Drive Pulses (5 μm cell gap).**



**Figure 5: Voltage Response Curve for 1.0 ms Conventional Drive Pulses (5 μm cell gap).**



**Figure 6: Reflectance vs. Gray Level for Nominal 45 V Reduction Pulses (60 Hz).**

is much less sensitive to pulse voltage, and thus is less sensitive to display imperfections as well.

Also apparent in Figures 4 and 5 is that it is not possible to drive from the planar initial state to the focal conic state with only one drive pulse of 0.5 ms or 1.0 ms. However, it is possible to apply pulses of these durations which drive the display towards slightly increased or decreased reflectance. Driving towards decreased reflectance is of more interest for these short drive pulses due to the high voltages required to increase reflectance. Because of the cumulative effect, multiple pulses may be applied to reduce the gray level to a desired level from an initially brighter level.

The amount of reduction in reflectance caused by each drive pulse may be controlled by adjusting the voltage of the pulse. Figure 4 shows that the maximum reduction in reflectance for 0.5 ms pulses occurs with pulse amplitudes near 70V, while Figure 5 shows that amplitudes near 40V cause the maximum reduction for 1.0 ms pulses. However, it is advantageous to minimize the cost of the drive electronics by fixing the drive voltage to a constant level. This is possible if variable width pulses are used. The reduction in reflectance of a 40V pulse of 0.5 ms is much different than that of a 40V pulse of 1.0 ms. It is thus possible to use pulses of fixed amplitudes and variable pulse widths to achieve a desired gray level reduction for each pulse.

The use of a direct drive architecture permits each pixel to be driven with pulses whose widths are independent of those applied to any other pixel. Additionally, the number of pulses applied to each pixel is independent of that of any other pixel. Generally, the cumulative effect has in the past been applied to achieve video rate scanning in displays addressed in a passive matrix. This restricts every pixel regardless of desired gray level to drive with the same number of pulses, each with the same pulse duration.

The final piece of the drive scheme is a method to reset a pixel to a uniform bright state. Figure 1 shows that this may be done by using a long drive pulse such as 100 ms with voltages as low as 30V. Resetting to the planar state poses no uniformity problems as the voltage response curve is flat at the pulse width and voltages used. Note that it is thus possible to create a drive scheme using just 1 voltage level (30V to 40V) in addition to zero. A long pulse would be used to reset to planar and short pulses to reduce the reflectance to the desired gray level. However, a higher voltage planar erase pulse is often desirable to speed up the update by reducing the duration of the planar erase.

**Table 1: Pulse Widths of Reduction Pulses.**

Pulse Number	Pulsewidth (ms)			
	20V (60 Hz)	30V (60 Hz)	45V (60 Hz)	45V (1 Hz)
1	1.10	0.68	0.45	0.44
2	1.08	0.60	0.44	0.44
3	0.95	0.60	0.44	0.47
4	0.98	0.58	0.43	0.44
5	0.95	0.62	0.44	0.50
6	0.98	0.64	0.45	0.50
7	1.08	0.67	0.49	0.52
8	1.12	0.70	0.50	0.56
9	1.12	0.70	0.52	0.58
10	1.16	0.72	0.52	0.58
11	1.30	0.80	0.60	0.61
12	1.40	0.87	0.62	0.66
13	1.60	1.10	0.76	0.76
14	1.95	1.30	0.86	0.86
15	2.50	1.50	1.00	1.00

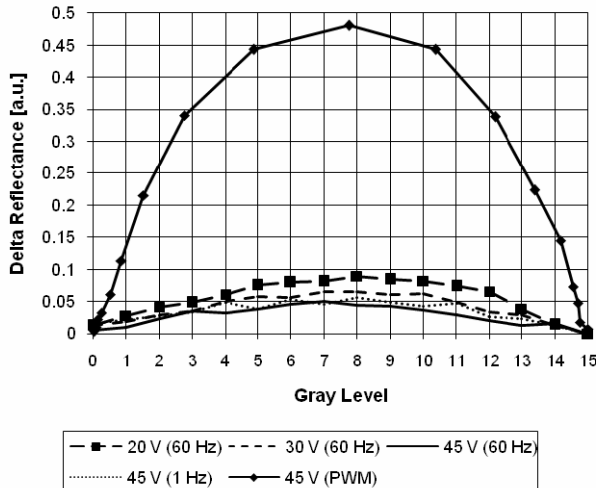
In simplest form, the proposed drive scheme thus consists of a planar erase pulse to bring the display to the brightest level, followed by a sequence of reduction pulses to decrease the reflectance to a desired gray level. The reduction pulses may all have the same amplitudes, but the pulse widths must be tuned to bring about the desired reduction in reflectance for each pulse. Generally, each pulse reduces the reflectance by one gray level. Reductions of more than one gray level are possible, but the longer pulse widths required may unnecessarily increase sensitivity. The final gray level is then determined by the number of pulses applied.

#### 4. Results and Discussion

The new drive scheme was implemented on the 5 $\mu$ m glass cell whose voltage response curves are given in Figures 1, 4, and 5. The drive waveforms consist of a 200 ms planar erase (50V, 250 Hz), a pause, and then from 1 to 15 reduction pulses to produce a total of 16 gray levels (the brightest level has no reduction pulses). Figure 6 illustrates the normalized reflectance of each gray level when 45V reduction pulses are used and the pulses are applied at a 60 Hz rate (each pulse begins 16.7 ms after the start of the previous pulse). Also shown is the reflectance resulting from 44V and 46V pulses. There is very little difference, especially when compared to the PWM scheme in Figure 3.

The pulse widths of the reduction pulses are given in Table 1. Pulse widths are tabulated for 20V, 30V, and 45V reduction pulses applied at a 60 Hz rate, as well as for 45V pulses applied at a 1 Hz rate. In each case the same planar erase was used, but the pause between the erase and the first pulse was 16.7 ms for the 60 Hz case and 1 s for the 1 Hz case. Pulse number 1 reduces the gray level from 15 to 14, pulse number 2 from gray level 14 to 13, and so on. In all instances, the overall trend is towards longer pulse widths at the darker gray levels.

The sensitivity of the new scheme for the four cases in Table 1 has been compared to the PWM approach. The procedure was to first tune each drive scheme to hit the sixteen gray levels at their nominal voltage of 20V, 30V, or 45V. The display was then driven to each of the gray levels using these drive parameters but with the voltage first increased and then decreased by 1/45 of the nominal voltage. The reflectance difference resulting from using the increased and decreased voltages at each gray level is a

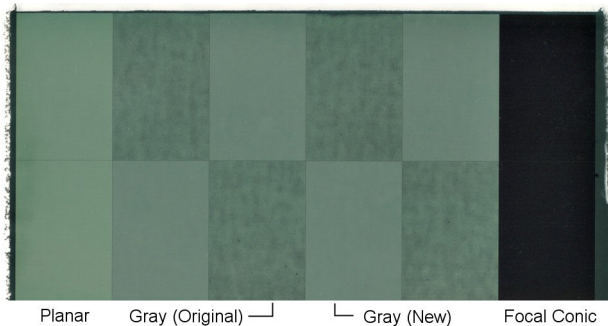


**Figure 7: Drive Scheme Sensitivity Comparison.**

measure of the sensitivity of the drive scheme to voltage and also to display imperfections.

The results are plotted in Figure 7. The PWM scheme clearly is much more sensitive at all gray levels than the pulsed scheme at any of the considered voltages. The pulsed scheme is least sensitive at 45V and most sensitive at 20V. This is expected as Table 1 indicates that lower voltage pulses require longer durations, which results in steeper, more sensitive voltage response curves.

Table 1 also shows a slight dependency of pulse width on pulse rate. At 45V, the 1 Hz pulse rate requires slightly longer pulses than at 60 Hz. However, the difference is small and so is the change in sensitivity as seen in Figure 7. The 60 Hz pulse rate is generally preferred if the display is to be viewed under 60 Hz AC lighting. Because the display is reflective, beat frequencies may be seen on the display if it is not driven in sync with an AC light source. This is not an issue with DC lighting or sunlight.



**Figure 8: Drive Scheme Comparison on Flexible Plastic Display.**

Figure 2 illustrates the visual effect of the new drive scheme. The bottom right pixel of this 9  $\mu\text{m}$  glass cell was driven from the planar texture with thirteen 45V reduction pulses with durations

between 0.36 ms and 1.10 ms. The difference from the previously described lower left pixel is dramatic.

The drive technique is equally applicable to flexible displays. Figure 8 illustrates similar results for a flexible display with 4.0  $\mu\text{m}$  cell gap made using the polymer induced phase separation (PIPS) approach. In this example, the original scheme pixels are driven from planar for 50 ms with a 26V pulse, while the new scheme pixels are driven from planar by five 0.4 ms pulses of 45V.

Many variations of the drive scheme are readily imaginable. For instance, short pulses of fixed duration and amplitude might be used, with multiple pulses used for each gray level. Gamma tuning would then be based on setting the number of pulses to achieve each gray level rather than pulse width. Also, as outlined here every update begins with a planar erase. It would be possible to implement reductions in gray level without the planar erase. The planar erase would then only be used when increases in gray level are required.

## 5. Conclusions

The new drive scheme developed in this work enables new applications of very low-resolution, large-area cholesteric displays to places such as architectural tiles and electronic skins for personalization of mobile devices. Large low-resolution displays can now exhibit near perfect gray levels without having to create a perfectly uniform display. This has the impact of reducing manufacturing constraints, thereby reducing the cost of the displays as well. The approach has been successfully applied to many various direct drive displays built on both rigid glass and flexible plastic substrates.

## 6. Acknowledgements

We would like to thank the State of Ohio and the Research and Commercialization Project for their grant support. We would also like to thank the entire team at Kent Displays, Inc. for their help in creating these incredible displays.

## 7. References

- [1] D.-K. Yang, J. W. Doane, *SID Intl. Symp. Digest Tech. Papers*, **23** 759 (1992).
- [2] D.-K. Yang, J. L. West, L.-C. Chien, J. W. Doane, *J. Appl. Phys.*, **76** 1331 (1994).
- [3] T. Schneider, F. Nicholson, A. Khan, J. W. Doane, L.-C. Chien, *SID Intl. Symp. Digest Tech. Papers*, **36** 1568 (2005).
- [4] S. Stephenson, D. M. Johnson, J. Kilburn, X.-D. Mi, C. M. Rankin, R. G. Capurso, *SID Intl. Symp. Digest Tech. Papers*, **35** 774 (2004).
- [5] J. W. Doane, D. Davis, A. Khan, E. Montbach, T. Schneider, I. Shyanovskaya, *Proc. Intl. Disp. Research Conf.*, **26** 9 (2006).
- [6] E. Montbach, D. Marhefka, D. J. Davis, M. Lightfoot, S. Green, N. Venkataraman, T. Schneider, A. Khan, J. W. Doane, *SID Intl. Symp. Digest Tech. Papers*, **37** 1737 (2006).
- [7] X.-Y. Huang, A. Khan, N. Miller, C. Jones, J. W. Doane, *Proc. Intl. Disp. Research Conf.*, **20** 30 (2000).